REMARKS

Upon entry of the present amendment, claims 1-20 are present and active in the application. No new matter has been added.

A widely used isolation technique in semiconductor structure, silicon trench isolation (STI) traditionally includes forming a screen SiO_2 layer on a semiconductor substrate, followed by depositing an isolation Si_3N_4 layer over the screen SiO_2. A photoresist is then deposited and the structure is etched, opening a trench in the substrate. The photoresist is stripped, an oxide layer is deposited, and the structure is planarized via CMP. The isolation Si_3N_4 layer is then etched away.

A problem with STI is the low uniformity of the surface after CMP, which renders overetching the isolation Si_3N_4 layer necessary in order to remove all the nitride. This results in a non-uniform thickness of the underlying screen SiO_2 layer, which negatively affects the consistency of the threshold voltages of the transistors on the wafer.

The present invention addresses this problem by providing an STI method that includes covering the semiconductor substrate with a new type of isolation region. As shown in Figure 6, this region has a first sacrificial oxide layer **118** over the screen SiO_2 layer **110**, and the isolation Si_3N_4 layer **106** over the sacrificial oxide layer. An optional second Si_3N_4 sacrificial layer **120** can also be part of the isolation region.

With this new type of structure, the first sacrificial layer protects the screen SiO_2 layer from the overetching of the isolation Si_3N_4 layer, thus leading to a product with a more uniform surface (page 4, line 20, to page 5, line 23).

As is clear from the specification and the figures, the word "on" in the present application and claims means "above" when the substrate is oriented to be at the bottom. This is the common use of the term, particularly in the context of semiconductor processing, where each subsequent layer formed is on the substrate.

The rejection of the claims over Lou et al. is respectfully traversed. The nitride layer of Lou et al. is not on the sacrificial layer.

Lou et al. provides a method where an isolation Si_3N_4 layer **14** is in contact with a screen SiO_2 layer **12** (Figure 1). An oxide layer **19** is present, which lines the trench, and lies over the SiO_2 layer **12** and the Si_3N_4 layer **14** (Figure 1). This layer is formed by thermal oxidation, and therefore forms only on exposed surfaces (col. 2, lines 442-48). At no point is the nitride layer **14** on this oxide layer **19**: the oxide layer **19** is adjacent and on the nitride layer **14**. After the etching and the deposition of the dielectric filler **20**, the structure of Lou et al. is subjected to a two-stage CMP step (col.2, lines 49-60) yielding the structure of Figure 2B which is then processed to the final product.

As claimed, the present invention includes a nitride layer on a sacrificial layer. As is clear from the specification and the figures, the word "on" in the present application and claims means "above" when the substrate is oriented to be at the bottom. In contrast, Lou et al. includes an oxide layer **19** which is formed after the nitride layer **14**, so that the nitride layer cannot be on the oxide layer **19**. Consequently, Lou et al. does not teach or suggest the method of the claimed invention. Withdrawal of these grounds of rejection are respectfully solicited.

The rejections of claims 20-22 have been obviated by the cancellation of these claims.

Applicants submit that the application is now in condition for allowance. Early notice of such action is earnestly solicited.

Respectfully submitted,

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